Fig.1

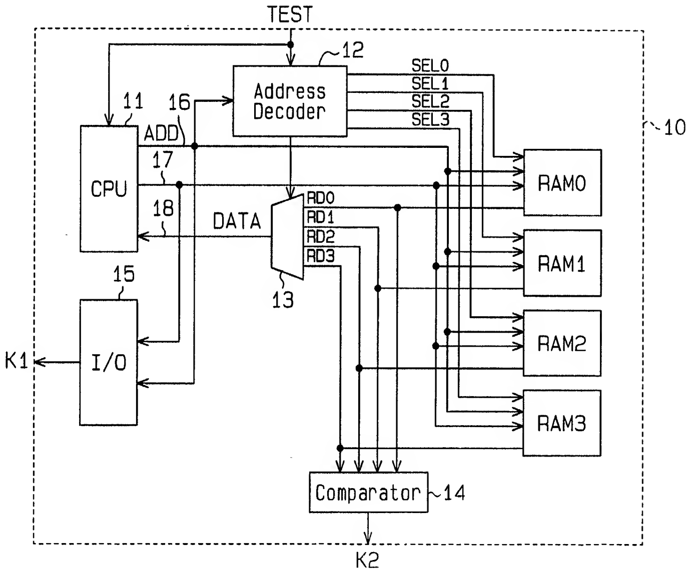

TEST
12
Address Decoder
SEL0
SEL1
SEL2
SEL3
10
11
16
ADD
CPU
17
18
DATA
RD0
RD1
RD2
RD3
13
RAM0
RAM1
RAM2
RAM3
15
I/O
K1
Comparator
14
K2

Fig.2

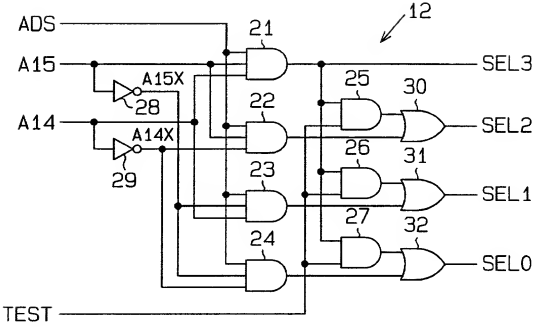


Fig.3

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	0
1	0	0	1	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1
0	X	X	X	0	0	0	0

Fig.4

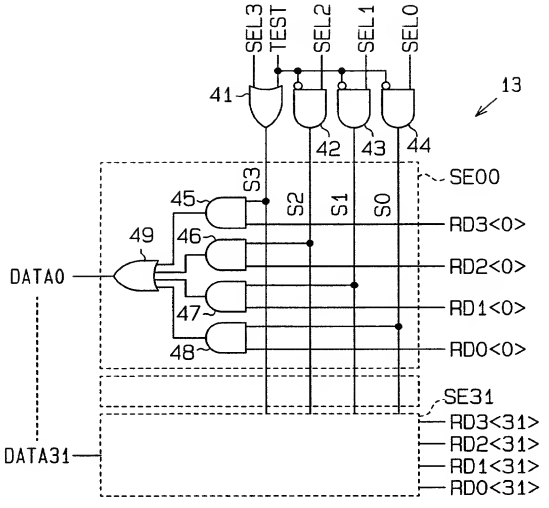

SEL3
TEST
SEL2
SEL1
SEL0
41
13
42
43
44
SE00
S3
S2
S1
S0
45
46
49
47
48
DATA0
RD3<0>
RD2<0>
RD1<0>
RD0<0>
SE31
DATA31
RD3<31>
RD2<31>
RD1<31>
RD0<31>

Fig.5

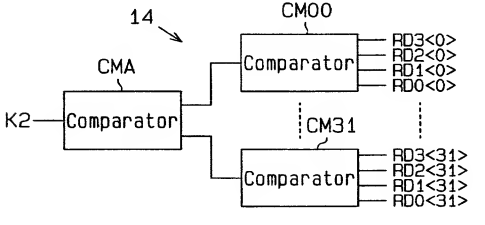

14
CM00
CMA
Comparator
RD3<0>
RD2<0>
RD1<0>
RD0<0>
K2
Comparator
CM31
Comparator
RD3<31>
RD2<31>
RD1<31>
RD0<31>

Fig.6

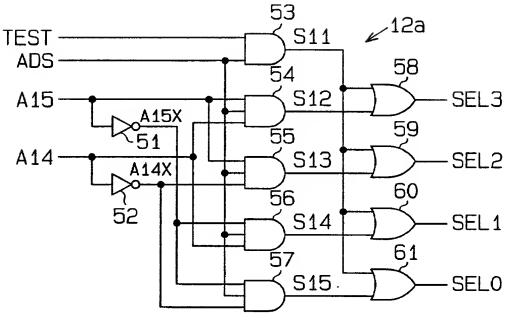


Fig.7

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	0
1	X	X	1	1	1	1	1
0	X	X	X	0	0	0	0

Fig.8

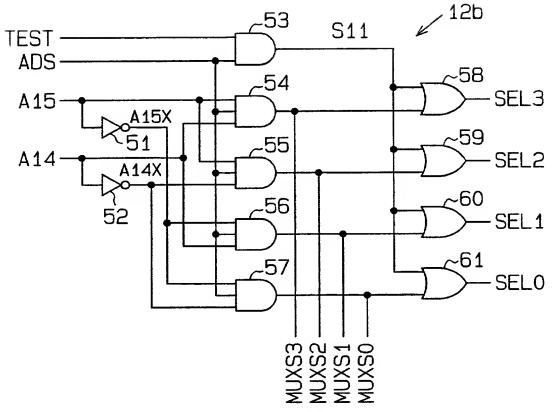


Fig.9

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	0
1	X	X	1	1	1	1	1
0	X	X	X	0	0	0	0

Fig.10

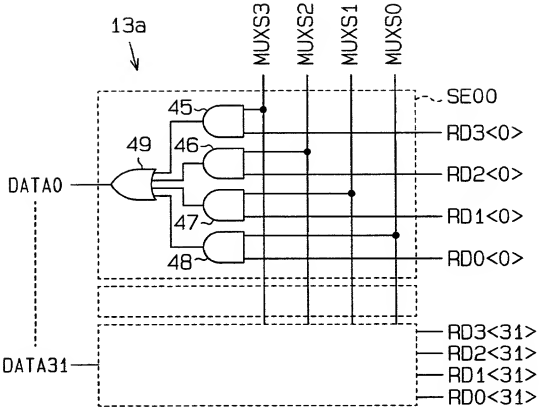

13a
MUXS3
MUXS2
MUXS1
MUXS0
SE00
45
46
47
48
49
DATA0
DATA31
RD3<0>
RD2<0>
RD1<0>
RD0<0>
RD3<31>
RD2<31>
RD1<31>
RD0<31>

Fig.11

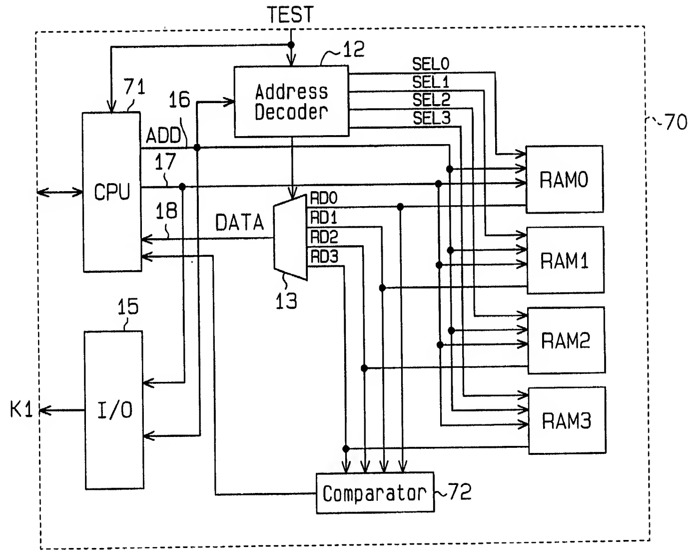

TEST
12
Address Decoder
SEL0
SEL1
SEL2
SEL3
71
16
ADD
17
CPU
18
DATA
RD0
RD1
RD2
RD3
13
RAM0
RAM1
RAM2
RAM3
70
15
I/O
K1
Comparator
72

Fig.12

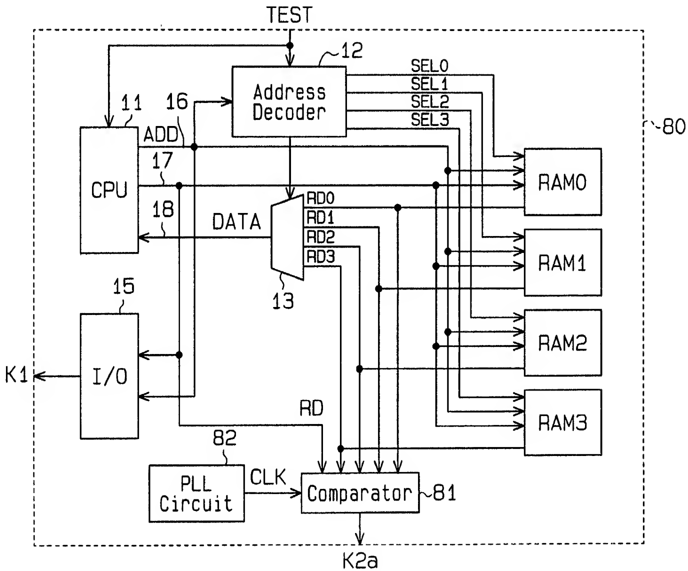

TEST
12
Address Decoder
SEL0
SEL1
SEL2
SEL3
80
11
16
ADD
CPU
17
18
DATA
RD0
RD1
RD2
RD3
13
RAM0
RAM1
RAM2
RAM3
15
I/O
K1
RD
82
PLL Circuit
CLK
Comparator
81
K2a

Fig.13

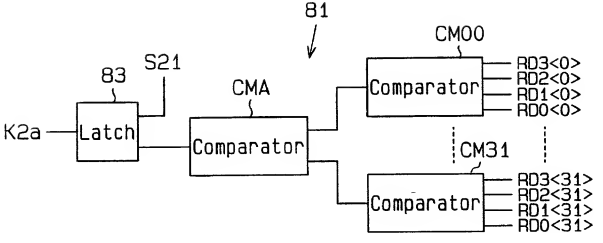

81
CM00
83
S21
CMA
Comparator
RD3<0>
RD2<0>
RD1<0>
RD0<0>
K2a
Latch
Comparator
CM31
Comparator
RD3<31>
RD2<31>
RD1<31>
RD0<31>

Fig.14

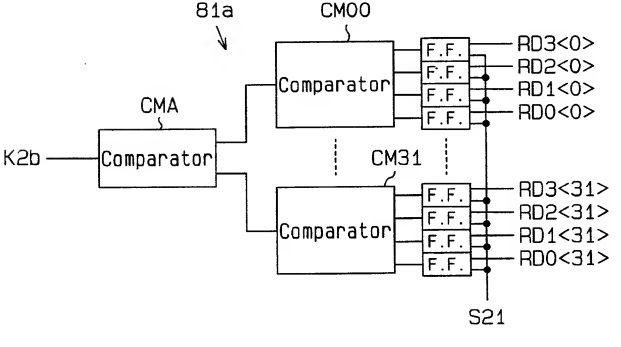
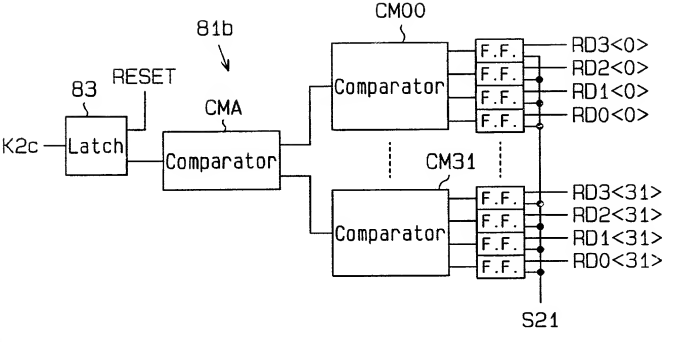

81a
CM00
F.F.
RD3<0>
RD2<0>
RD1<0>
RD0<0>
Comparator
CMA
K2b
Comparator
CM31
Comparator
RD3<31>
RD2<31>
RD1<31>
RD0<31>
S21

Fig.15


81b
CM00
RESET
83
CMA
K2c
Latch
Comparator
Comparator
CM31
Comparator
F.F.
F.F.
F.F.
F.F.
F.F.
F.F.
F.F.
F.F.
RD3<0>
RD2<0>
RD1<0>
RD0<0>
RD3<31>
RD2<31>
RD1<31>
RD0<31>
S21